Modeling and Analysis of a Nonlinear Adaptive Filter Control for Interline Unified Power Quality Conditioner

[1]Tahsin Köroğlu, [2]Mustafa İnci, [3]K. Çağatay Bayındır, [4]Mehmet Tümay

[1] Osmaniye Korkut Ata University, Department of Electrical and Electronics Engineering, Osmaniye, TURKEY
[2, 3, 4] Çukurova University, Department of Electrical and Electronics Engineering, Adana, TURKEY

[1]tkoroglu@osmaniye.edu.tr, [2]minci@cu.edu.tr, [3]cbayindir@cu.edu.tr, [4]mtumay@cu.edu.tr

***Abstract*—In this paper, one of the known interline custom power devices named Interline Unified Power Quality Conditioner (IUPQC) is improved for various power quality disturbances and modeled in PSCAD/EMTDC. The developed topology can be used for simultaneous compensation of voltage and current imperfections in a multibus/multifeeder system. The proposed IUPQC is designed for medium voltage level (11 kV) and effective Enhanced Phase Locked Loop (EPLL) based control technique is used to detect and extract the PQ disturbances. The performance of Series Compensator of IUPQC is evaluated through extensive simulations for mitigating unbalanced voltage sags with phase jumps and interruption. The performance of Shunt Compensator of IUPQC is also tested for harmonic and reactive power compensation that are not investigated before in literature. It is verified that IUPQC which is connected to two feeders, can compensate current and voltage distortions succesfully in these feeders according to the results obtained using PSCAD/EMTDC.**

Keywords-Interline Unified Power Quality Conditioner, Custom Power, Power Quality, Enhanced Phase Locked Loop

I. INTRODUCTION

In recent years, the use of nonlinear and electrically switched devices that draw non-sinusoidal currents in to the power systems have increased in utility and thus contribute to the degredation of power quality. Power quality problems such as harmonics, voltage sag/swell, interruption, imbalance, transients and flicker have become serious concern for both electric utility companies and electric power consumers. On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation [1].

Custom power is a technology-driven product and service solution which embraces a family of devices to provide power-quality enhancement functions [2]. Custom power devices that are based on the voltage source converter (VSC) are increasingly used for applications such as active filtering, load balancing, power factor correction and voltage regulation in distribution systems [3]. The most well-known custom power devices are the Active Power Filter (APF), the Distribution Static Compensator (DSTATCOM), the Dynamic Voltage Restorer (DVR), the Static Transfer Switch (STS) and the Unified Power Quality Conditioner (UPQC) [4].

In recent studies, the concept of the multiconverter based Interline Custom Power Devices are introduced. In an interline custom power device, two or more VSCs are connected back-to-back through a common dc capacitor to two neighboring feeders. These devices can be of series-series, shunt-shunt or series-shunt type [5]. The main advantage of multi-feeder devices is that if any power quality problem occurs in one feeder, other adjacent feeder supplies power for compensating power quality problem. Therefore the multi-feeder PQ devices assure superior performance than single feeder PQ devices.

The first interline custom power device called as Interline DVR (IDVR) is proposed in [2,6]. An IDVR consists of two DVRs both supplied from a common DC link and connected to different distribution feeders in the power distribution system. One of the DVRs compensates for the voltage sag while the other DVR maintains the DC link voltage to a specific level by absorbing real power from the AC system [7-10]. Borrowing the idea of IDVR, some additional devices that operate in multi-feeder systems have been proposed; one of these devices is Interline Voltage Controller (IVOLCON) which is mentioned in [5,11]. IVOLCON consists of two shunt voltage source converters (VSCs) that are joined through a common dc bus and connected to different distribution feeders in the power distribution system. The main aim of the IVOLCON is to control the two PCC (point of common coupling) bus voltages of the two feeders to prespecified magnitudes with mutual support by providing bi-directional power flow through the dc link. Using the prevailing idea of the concepts of IDVR and IVOLCON, a new concept named the Interline Unified Power Quality Conditioner (IUPQC) has been proposed in [3]. This concept can also be considered as the implementation of known Unified Power Quality Conditioner (UPQC) structure in two different feeders. The purpose of IUPQC is to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. Multiconverter United Power Quality Conditioner (MC-UPQC) is the most recent interline custom

978-1-4673-6392-1/13/$31.00 ©2013 IEEE

power device which is proposed in [1]. In the basic configuration of MC-UPQC, one shunt and two series VSC exist. The MC-UPQC system can be applied to adjacent feeders to compensate for supply voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeder [1].

This study mainly focuses on modeling of IUPQC in PSCAD/EMTDC simulation pragram. The proposed IUPQC is designed for medium voltage level (11 kV) and is developed for simultaneous compensation of voltage and current distortions in a multifeeder system. An effective EPLL based control technique is used for IUPQC to detect and extract the PQ disturbances. The performance of proposed IUPQC system is evaluated through extensive case studies for mitigating harmonics, unbalanced voltage sags with phase jumps and interruption. The paper is organized in the following manner: System description, power circuit configuration and control strategy of proposed IUPQC are presented in section 2. Simulation results for different case studies are provided and discussed in section 3. Finally, conclusions of the study are given in section 4.

II. PROPOSED IUPQC SYSTEM

A. System Description

The structure of the IUPQC connected to a distribution system is shown in Fig. 1. As shown in this figure, the feeder impedances are denoted by (R_{s1}, L_{s1}) and (R_{s2}, L_{s2}). It can be seen that two feeders Feeder-1 and Feeder-2 are connected to two different substations that supply the system loads L1 and L2. The IUPQC is connected to two buses BUS1 and BUS2 with voltages u_{bus1} and u_{bus2}. The supply voltages are denoted by u_{s1} and u_{s2} while load voltages are denoted by u_{l1} and u_{l2}. Finally, two feeder currents are denoted by i_{s1} and i_{s2} while load currents are denoted by i_{l1} and i_{l2}.

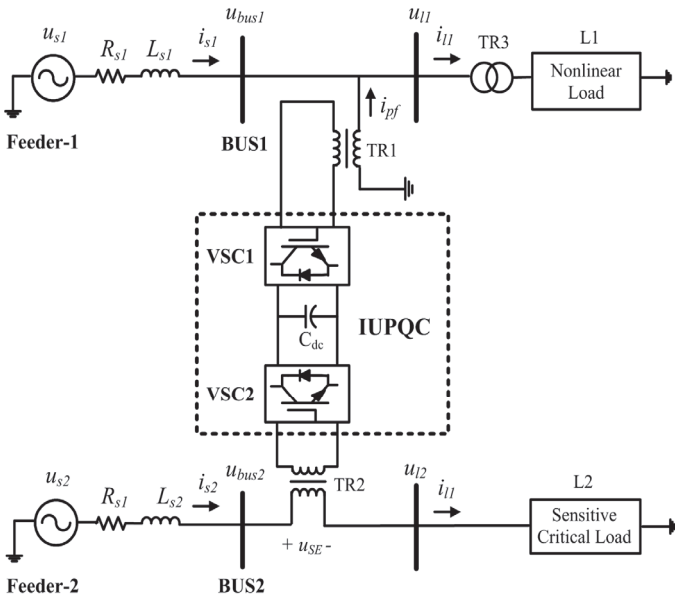

Figure 1. The Structure of IUPQC connected to distribution system

The IUPQC consists of one series and one shunt converter which are connected to two adjacent feeders with being supplied from a common DC link. This topology provides power transfer between two adjacent feeders through DC link and it is very advantageous instead of conventional UPQC topology in a single feeder. In the proposed configuration, VSC1 is connected in parallel with load L1 at the end of Feeder-1 and VSC2 is connected in series with BUS2. The aims of the IUPQC are listed below:

1) to compensate for reactive and harmonic components of nonlinear load current (i_{l1});
2) to regulate the load voltage (u_{l2}) against sag/swell, interruption and disturbances in the system to protect the sensitive/critical load L2.

In order to achive these two goals, shunt VSC (VSC1) operate as a current controller while the series VSC (VSC2) operate as a voltage controller.

B. Power Circuit Configuration

The IUPQC shown in Fig. 1 consists of two VSCs (VSC1 and VSC2) that are connected back to back through a common dc capacitor (C_{dc}). In this topology VSC1 is connected in shunt to Feeder-1 while the VSC2 is connected in series with Feeder-2. The components of shunt compensator power circuit are DC link capacitor, three-phase inverter circuit and smoothing inductor ($L_{f,apf}$) as shown in Fig. 2.

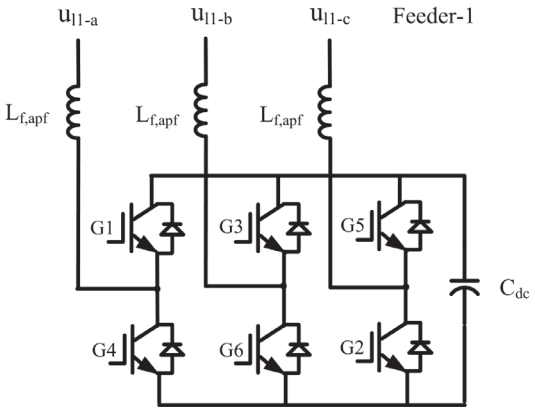

Figure 2. The schematic structure of Shunt VSC (VSC1)

Three-phase three-wire voltage source inverter topology is used as shunt compensator in this study. The smoothing inductors establish a link between VSC1 and power system. Smoothing inductors convert VSC voltage to current and allow shunt compensator to act as a current source. DC capacitor (energy storage unit) supplies required power for harmonic compensation of load current during operation. DC link voltage must be higher than the peak value of the utility voltage; otherwise the generated compensation currents cannot be injected to the power system. The shunt compensator must be connected to 11 kV level via transformer because of the limits of power semiconductor devices in VSC.

The components of series compensator power circuit are DC link capacitor, inverter circuit, inverter side filter and injection transformer as shown in Fig. 3.

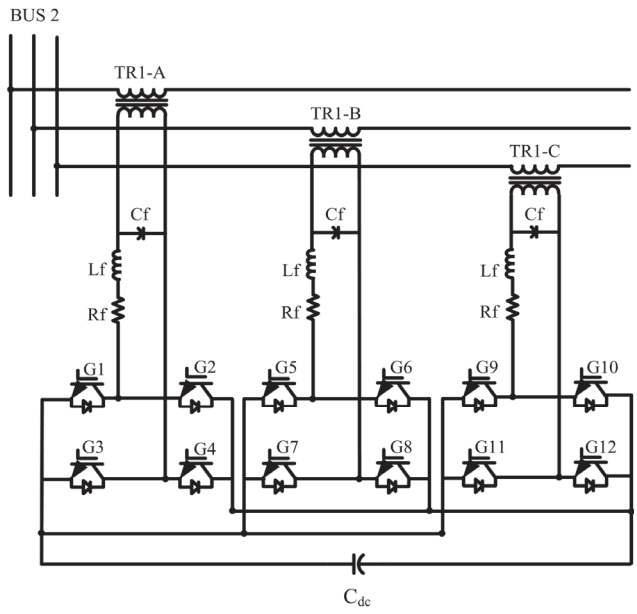

Figure 3. The schematic structure of Series VSC (VSC2)

Three single-phase H-Bridge voltage source inverter topology is used as series compensator in this study. Use of single-phase H-bridge PWM inverters makes possible the injection of positive, negative and zero sequence voltages. Thus, H-bridge PWM switched inverters provide superior performance to control asymmetries during unbalanced faults. The Series Compensator of IUPQC are connected to the distribution system in series through single phase injection transformers. The injection transformer primary winding is connected with series compensator power circuit while its secondary winding is connected in series with the distribution line. The main purpose of the injection transformer is to boost the voltage supplied by the filtered VSC output to the desired level while isolating the Series Compensator circuit from the distribution network [12]. In this study, LC type inverter side filter is used to attenuate the high-order harmonics generated by the voltage source inverter. Inverter side filtering scheme has the advantage of being closer to the harmonic source thus high-order harmonic currents are prevented to penetrate in to the series injection transformer thus necessitates a lower rating on the injection transformer [13].

C. Control Strategy

The IUPQC consist of Shunt and Series VSC which are controlled independently. The switching control strategy for series VSC and the shunt VSC are selected to be sinusoidal pulsewidth modulation (PWM) voltage control and hysteresis current control, respectively. In this study, simple and effective control algorithm is used to detect and extract the PQ disturbances. The algorithm is based on the nonlinear adaptive filter named Enhanced Phase Locked Loop (EPLL) presented in [14]. The reason of preferring EPLL is that it has simple structure than most preferred time based and frequency based methods and it has fast and accurate response with changing load conditions.

The EPLL is inherently adaptive and follows variations in amplitude, phase angle and frequency of the input signal. The EPLL is capable of accurately estimating the fundamental component of a polluted signal. The structure of the EPLL shown in Fig. 4, is simple and this makes it suitable for real-time embedded applications for software or hardware implementation [15]. The EPLL is formed from three main parts as shown in Fig. 4. These mainparts are phase detector (PD), low pass filter (LPF) and voltage controlled oscillator (VCO). The EPLL receives the input signal *u(t)* and provides an on-line estimate of the following signals:

- The synchronized fundamental component, *y(t)*;
- The amplitude, *A(t)* of *y(t)*;
- The difference of input and synchronized fundamental component, *e(t)*;
- The frequency deviation, *Δw(t)*;
- The phase angle *θ(t)* of *y(t)*.

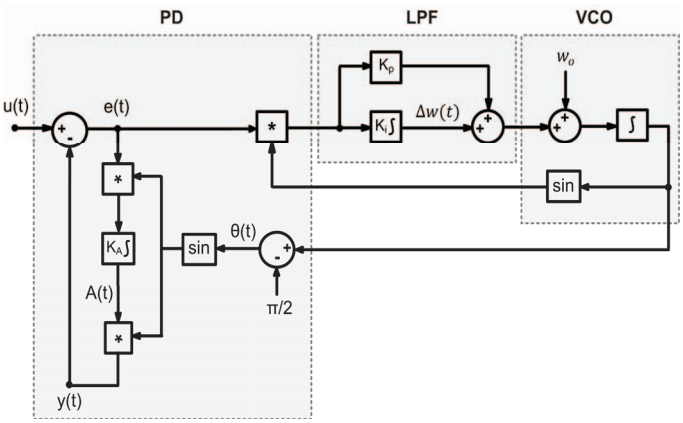

Figure 4. The structure of EPLL and its parameters

Mathematically, the EPLL is described by three main differential equations in time domain:

$$A(t) = \int e(t).\sin\theta(t).K_A.dt \quad (1)$$

$$\Delta wt = \int e(t).\sin(\theta + \pi/2)(t).K_i.dt \quad (2)$$

$$\theta(t) = -\pi/2 + \int [e(t).\cos\theta(t).K_p + \Delta wt + w_o]\,\mathrm{d}t \quad (3)$$

The error signal, $e(t) = u(t) - y(t)$, is the total distortion signal of the input and can be expressed as a continuous time;

$$e(t) = u(t) - \sin\theta(t)\int e(t).\sin\theta(t).K_A.dt \quad (4)$$

K_A, K_i and K_p are gains and time constants of integrals that can affect the lock time of loop, amplitude estimation time and phase accuracy of input signal [15].

Functions of the shunt VSC (VSC1) are to compensate for the reactive component of load L1 current (i_{l1}), to compensate for the harmonic components of i_{l1} and to regulate the voltage of the common dc capacitor (V_{cap}). The controller algorithm of shunt compensator is formed from the harmonic current extraction, hysteresis current controller, DC link voltage controller and reactive power control as shown in Fig. 5.

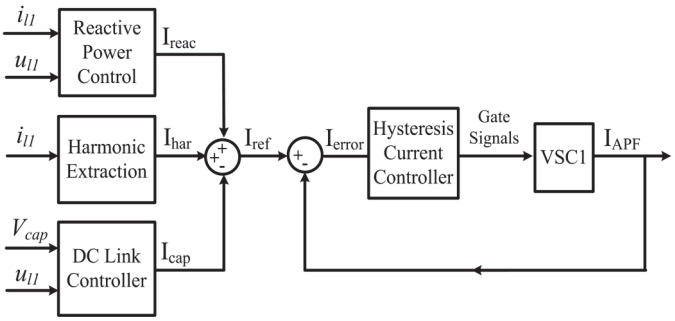

Figure 5. The control algorithm of Shunt Compensator

Shunt Compensator control system measures the load voltages (u_{ll}), dc capacitor voltage (V_{cap}), load currents (i_{ll}) and injected currents (I_{APF}). The controller processes the measured values and generates the required compensation signals. These signals are then compared in hysteresis controller and the required gate signals are generated.

When the distorted current or voltage signal is applied to EPLL, the harmonics and interharmonics of distorted signal (I_{har}) can be obtained from the *e(t)* signal of EPLL. DC link voltage control is achieved by using PI controller. The input of the PI controller is the error between the actual capacitor voltage V_{cap} and its reference value $V_{cap,ref}$. In order to keep DC link voltage at a constant level, shunt compensator must draw active power by drawing current (I_{cap}) in phase with line voltage. To draw a current in the same phase with system voltage, phase information of system voltage (δ_{Vload}) must be known. This can be achieved by using EPLL. With using phase of system voltage, DC link control reference current signal is created by multiplying the PI controller output and sine wave created by phase information of system voltage. The block diagram of reactive power control used in control method of Shunt Compensator module (VSC1) is shown in Fig. 6 [15]. Two identical EPLL units are used for voltage and current signals. The top portion of the unit is used for voltage and the bottom portion is used for current signal processing. The link between the two parts is to calculate the fundamental reactive current component (I_{reac}).

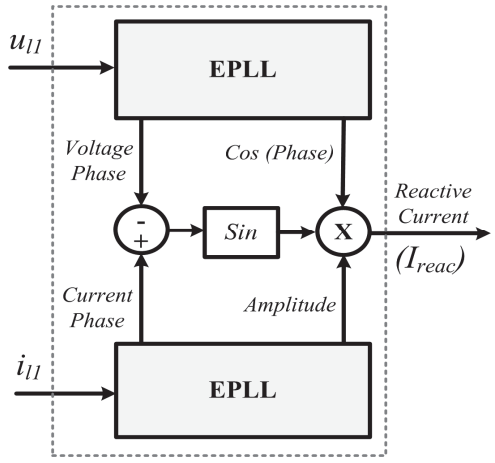

Figure 6. Block diagram of the proposed reactive-current extraction unit

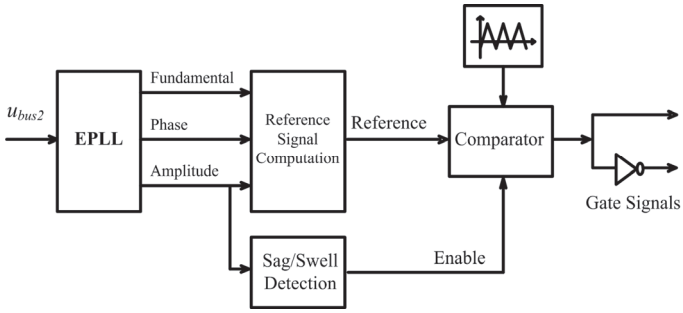

Figure 7. The control algorithm of Series Compensator

The main aim of the series VSC (VSC2) is to mitigate voltage sag/swell and interruption in Feeder-2. The control system of series compensator consists of sag/swell detection, reference voltage extraction and gate signal generation as shown in Fig. 7.

Simple and effective control algorithm is proposed for both sag/swell detection and reference voltage generation in this paper. The algorithm is based on the EPLL that extracts and directly provides the amplitude *A(t)*, phase angle *θ(t)* and fundamental component *A(t) cosθ(t)* of the input signal for each phase independently. With the proposed method, the controller is able to detect balanced, unbalanced and single phase voltage sags/swells without an error. In this method, three EPLLs are used to track each of the three phases.

In the EPLL, the measured phase supply voltages are converted to per unit value. *A(t)* gives the amplitude of the tracked signal *u(t)*. If there is no sag or swell, *A(t)* signal is obtained as continuous 1 pu. By subtracting the *A(t)* signal from the ideal voltage magnitude (1 pu), the voltage sag/swell depth (S_{depth}) can be detected. The comparison of this value with the limit value of 10% (0.1 pu) gives information whether a fault occurred or not [16]. The voltage sag/swell detection based on EPLL method is presented in Fig. 8.

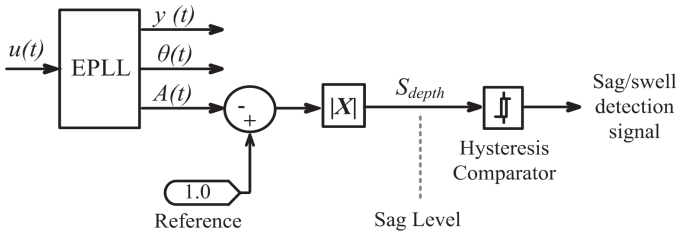

Figure 8. Block diagram of proposed EPLL based sag detection method

Reference voltage V_{error} is calculated according to voltage injection strategy by using magnitude *A(t)*, the output *y(t)* and phase *θ(t)* signals extracted with EPLL. In this study, Pre-Sag Compensation method is used as voltage injection strategy. Pre-Sag Compensation (PSC) method tracks supply voltage continuously and if it detects any disturbances in supply voltage it will inject the difference voltage ($V_{error,\ presag}$) between the sag or voltage at point common coupling (PCC) and pre-fault condition, so that the load voltage can be restored back to the pre-fault condition.

If sag is accompanied by a phase jump, PSC method offers better performance by compensating voltage sags in the both phase angle and amplitude for sensitive loads [17]. Other voltage injection strategies such as in-phase, phase-advance and minimum energy injection compensation methods may not prevent the phase jump of the load voltage at the starting and ending instants of the sag compensation period [18].

PWM switching method is used as gate signal generation for series converter. The switching pulses are generated by comparing the reference voltage compensation signal V_{error} with a fixed frequency carrier triangular wave.

III. SIMULATION RESULTS

The proposed IUPQC and its control schemes are tested through extensive case study simulations. In this section, simulation results obtained by PSCAD/EMTDC are presented, and the performance of the proposed IUPQC is analyzed. The system parameters of IUPQC system are provided in Table 1 and EPLL parameters are given in Table 2.

TABLE I. SYSTEM PARAMETERS

System Parameters	Values
Fundamental Frequency (*f*)	50 Hz
Voltage Source (u_{s1})	11 kV (L-L, rms), phase angle 0°
Voltage Source (u_{s2})	11 kV (L-L, rms), phase angle 0°
Feeder-1 ($R_{s1}+j2\pi fL_{s1}$)	Impedance: 0,0015+j0,0785 Ω
Feeder-2 ($R_{s2}+j2\pi fL_{s2}$)	Impedance: 0,0015+j0,0785 Ω
Nonlinear Load (*L1*)	A three-phase diode bridge rectifier that supplies a load of 100+j125.66 Ω
Sensitive/Critical Load (*L2*)	150.0+j23.56 Ω
DC Link Capacitor (C_{dc})	40 mF
DC Capacitor Voltage (V_{cap})	1700 V
Coupling Transformer (TR1)	2 MVA, 11/1 kV Δ/Y, Uk: 5%
Injection Transformer (TR2)	2 MVA, 1.2/8.0 kV, 10% Leakage reaktance
Power Transformer (TR3)	2 MVA, 11/6.3 kV Δ/ Δ, Uk: 10%

TABLE II. EPLL PARAMETERS

Parameters	Values
Integral Time Constant	0.02 s
K_A	500
K_i	30
K_p	300

A. Harmonic Distortion on Feeder-1

This case presents how VSC1 overcomes the load current harmonics with the proposed control algorithms. A three-phase diode bridge rectifier is used as a harmonic current producing load. The nonlinear load contains lower and higher order harmonics with a total value of 25.08% THD before compensation. VSC1 eliminates the load current harmonics by injecting current that cancel harmonic currents of nonlinear load as shown in Fig. 9. The waveforms indicate the nonlinear load current (I_{l1}), its corresponding compensation current injected by VSC1 (i_{pf}), compensated Feeder-I current (i_{S1}) and the dc link capacitor voltage (V_{cap}) of Phase-A respectively. The results show that a successful reduction in harmonics of the nonlinear load current (i_{l1}) is obtained. A nonlinear load current with 25.08% THD is reduced to less than 5%. The PI controlled dc-link capacitor voltage is nearly kept at 1.7 kV.

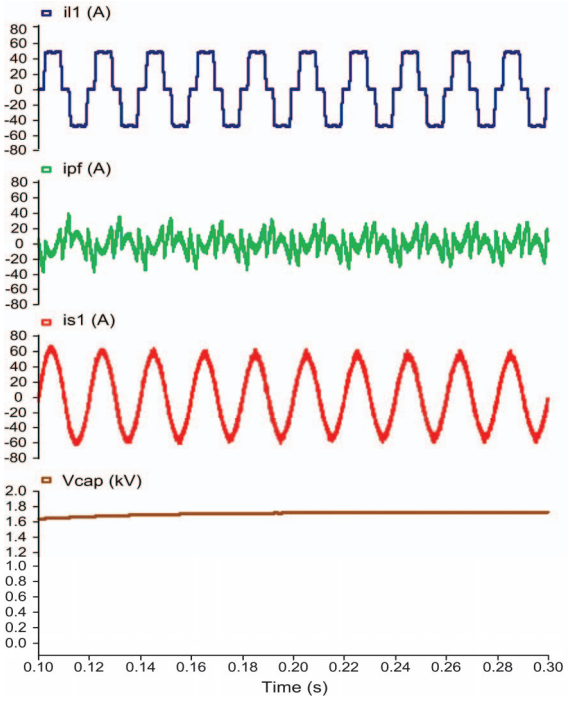

Figure 9. Nonlinear load current, compensating current, Feeder1 current and dc link capacitor voltage for Case A

B. Voltage Sag on Feeder-2

In this case, single line-to-ground unbalanced fault is considered, since it is most likely to occur in 70% of among all voltage sags in a distribution system [16]. 35% Single line-to-ground fault with 47.64o phase angle jump is investigated which occurs on Phase-A of BUS2 voltage between 0.3 s < t < 0.5 s. The sensitive/critical load (L2) voltage is not affected by voltage sag with the help of series compensator (VSC2). Fig. 10 shows the BUS2 voltage (u_{bus2}), series compensating voltage (u_{SE}), L2 load voltage (u_{l2}) and dc link capacitor voltage (V_{cap}).

C. Upstream Fault on Feeder-2

In this case study, the performance of VSC2 for upstream fault (interruption) mitigation on Feeder-2 is investigated. Single phase (L-G) interruption occurs on Phase-A of BUS2 voltage between 0.6 s < t < 0.8 s, and 25.27° phase angle jump occurs during the interruption. The sensitive/critical load (L2) voltage is not affected by voltage sag with the help of series compensator (VSC2). Fig. 11 shows the BUS2 voltage (u_{bus2}), series compensating voltage (u_{SE}) and L2 load voltage (u_{l2}) and the dc link capacitor voltage (V_{cap}).

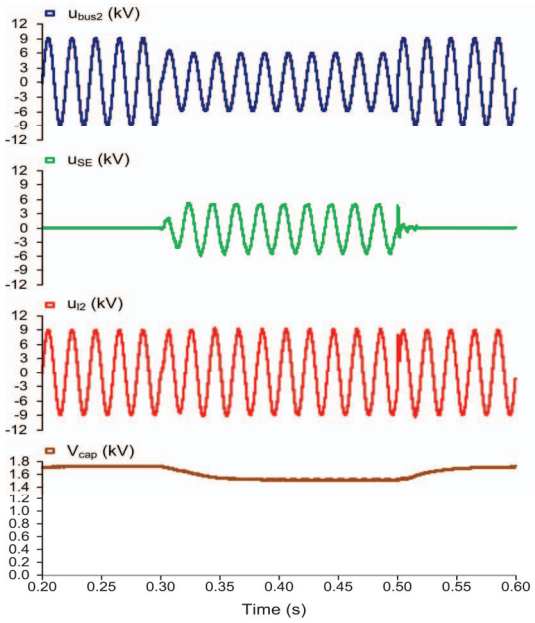

Figure 10. BUS2 voltage, series compensating voltage, load (L2) voltage and dc link capacitor voltage for Case B

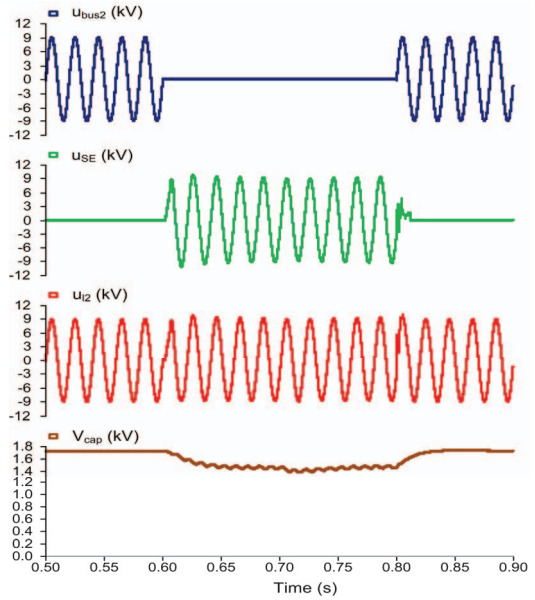

Figure 11. BUS2 voltage, series compensating voltage, load (L2) voltage and dc link capacitor voltage for Case C

IV. CONCLUSION

In this paper, an improved IUPQC topology for simultaneous compensation of voltage and current in adjacent feeders has been proposed. An effective EPLL based control technique is used for IUPQC to detect and extract the PQ disturbances in multi-feeder system. Each phases of Series and Shunt Compensator are investigated independently with EPLL based controller. The performance of proposed IUPQC system is evaluated through extensive simulations for mitigating harmonics, unbalanced voltage sags with phase jumps and interruptions. The results of simulations show its effectiveness in handling these PQ issues, so that smooth and clean power flow to the loads.

REFERENCES

[1] H. R. Mohammadi, A. Y. Varjani and H. Mokhtari, "Multiconverter Unified Power-Quality Conditioning System: MC-UPQC," IEEE Transactions on Power Delivery, vol. 24, no. 3, July 2009.

[2] M. D. Vilathgamuwa, D. Wijekon, S. Choi, "A Novel Technique to Compensate Voltage Sags in Multiline Distribution System - The Interline Dynamic Voltage Restorer," IEEE Transactions on Industrial Electronics, vol.53, no:5, pp.1603-1611, 2006.

[3] A. K. Jindal, A.Ghosh, A. Joshi, "Interline Unified Power Quality Conditioner," IEEE Transactions on Power Delivery, vol. 22, no: 1, January 2007.

[4] H. Kian, C. Yun, L. Ping, "Model-Based H∞ Control of a Unified Power Quality Conditioner," IEEE Transactions on Industrial Electronics, vol.56, no:7, pp.2493-2504, 2009.

[5] A.K. Jindal, A. Ghosh, A. Joshi and A. M. Gole, "Voltage Regulation in Parallel Distribution Feeders Using IVOLCON," Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, IEEE, 2008.

[6] D. M. Vilathgamuwa, H. M. Wijekoon and S. S. Choi, "Interline Dynamic Voltage Restorer: A Novel and Economical Approach for Multiline Power Quality Compensation," IEEE Transactions on Industry Applications, vol. 40, no. 6, 2004.

[7] M. R. Banei, S. H. Hosseini and G. B Gharehpetian, "Inter-line Dynamic Voltage Restorer Control Using a Novel Optimum Energy Consumption Strategy," Simulation Modelling Practice and Theory, vol. 14, Elsevier, 2006.

[8] H. R. Karshenas and M. Moradlou, "Design Strategy for Optimum Rating Selection in Interlıne DVR," Canadian Conference on Electrical and Computer Engineering, IEEE, 2008.

[9] C. N. Ho and H. S. C. Chung, "Implementation and Performance Evaluation of a Fast Dynamic Control Scheme for Capacitor-Supported Interline DVR" IEEE Transactions on Power Electronics, vol. 25, no. 8, 2010.

[10] M. Moradlou and H. R. Karshenas, "Design Strategy for Optimum Rating Selection of Interline DVR," IEEE Transactions on Power Delivery, vol. 26, no. 1, 2011.

[11] A. K. Jindal, A. Ghosh and A. Joshi, "Power Quality Improvement Using Interline Voltage Controller," IET Generation Transmission & Distribution, vol.1, no. 2, 2007.

[12] K. Perera, A. Atputharajah, S. Alahakoon and D. Salomonsson, "Automated control technique for a single phase dynamic voltage restorer," Proceedings of the International Conference on Information and Automation, Colombo, Sri Lanka, 2006.

[13] S. Choi, B. H. Li, D. Vilathgamuwa, "Design and Analysis of the Inverter-Side Filter Used in the Dynamic Voltage Restorer," IEEE Transactions on Power Delivery, vol. 17, no. 3, pp. 857-864, 2002.

[14] M. Karimi-Ghartermani and M. R. Iravani, "A Nonlinear Adaptive Filter for Online Signal Analysis in Power Systems Applications," IEEE Transactions on Power Delivery, vol. 17, pp. 617-622, 2002.

[15] M. Karimi Ghartemani, M. R. Iravani and F. Katiraei, "Extraction of Signals for Harmonics, Reactive Current and Network-Unbalance Compensation," IEE Proceedings Generation, Transmission and Distribution, vol. 152, no. 1, pp. 137-143, 2005.

[16] A. Teke, L. Sarıbulut and M. Tümay, "A Novel Reference Signal Generation Method for Power-Quality Improvement of Unified Power-Quality Conditioner," IEEE Transactions on Power Delivery, vol. 26, no.4, pp. 2205-2214, 2011.

[17] J. G. Nielsen, F. Blaabjerg and N. Mohan, "Control Strategies for Dynamic Voltage Restorer Compensating Voltage Sags with Phase Jump," Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2001.

[18] V. K. Ramachandaramurthy, A. Arulampalam, C. Zhan, M. Barnes amd J. Jankins, "Control of a Battery Supported Dynamic Voltage Restorer," IEE Proceedings Generation, Transmission and Distribution, vol. 149, no. 5, pp. 533-542, 2002.